USN	

10EC077

M.Tech. Degree Examination, June/July 2011 Synthesis and Optimization of Digital Circuits

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions.

- a. Draw Gajski and Kuhn's y-chart for synthesis task involved at each level with examples. 1
 - b. Explain circuit optimization at the architectural level with an example using design evaluation space. (06 Marks)
 - c. Explain briefly semicustom design.

(04 Marks)

a. Explain the characteristic numbers of a graph and find whether the graph shown in Fig.Q2(a) is perfect or not. (07 Marks)

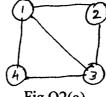


Fig.Q2(a)

b. Prove that LEFT EDGE algorithm is exact.

(07 Marks)

c. Explain Bryant's reduction algorithm.

(06 Marks)

- a. Write i) VHDL and ii) UDL/I code for finite state machine that recognizes two or more 3 consecutive is in an input data stream. (08 Marks)
 - b. Explain briefly dataflow and sequencing graphs with example.

(06 Marks)

c. Explain anatomies of software and hardware compilers.

(06 Marks)

- a. Explain Expand, Reduce, Reshape and irredundant operators with example for Leuristic Logic minimization. (10 Marks)
 - b. Explain encoding algorithm with example.

(10 Marks)

5 a. Explain algebraic substitution algorithm with example.

(10 Marks)

b. A logic network is specified by the following expressions:

$$f_x = ace + bce + de + g$$

$$f_v = ad + bd + cde + ge$$

$$f_z = abc$$

Generate all kernels and co-kernels of the above expressions. Extract single cube and multiple cube subexpressions. (10 Marks)

a. Explain state encoding problem for two level circuits with example.

(10 Marks)

b. Discuss FEAS algorithm with an example.

(10 Marks)

a. Discuss the ALAP scheduling algorithms with example.

- b. Write the pseudo-code of a list scheduler for the minimum-latency problem under resource and relative timing constraints. (10 Marks)
- 8 Write short notes on:
 - a. FPGA

- b. Simulators for digital design
- c. DFT techniques

c. Automatic test pattern generators. (20 Marks)